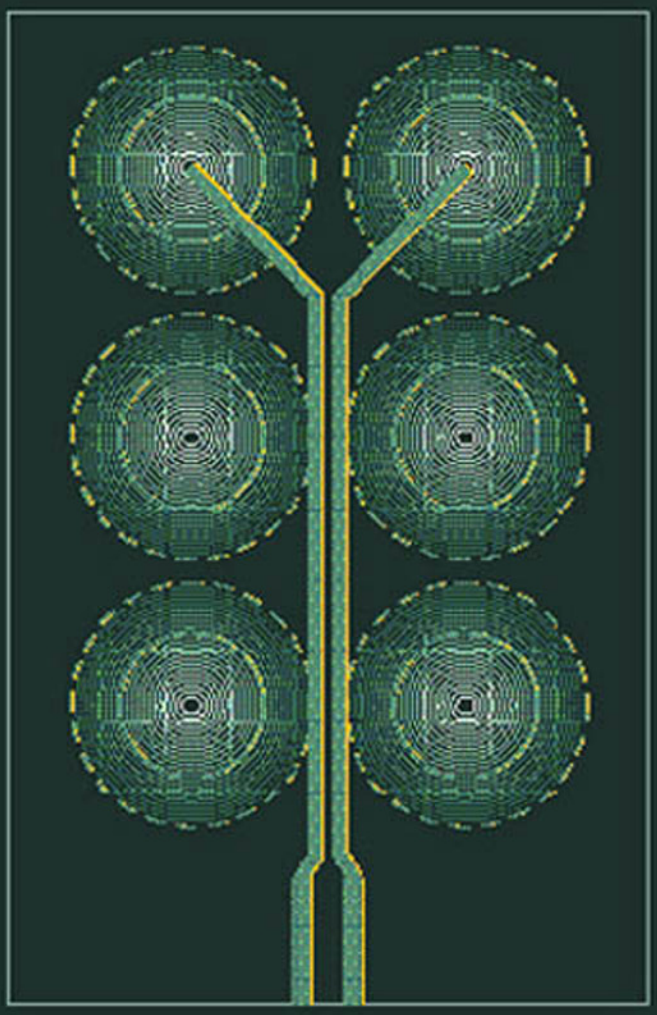
STEPHEN C. THIERAUF



HIGH-SPEED CIRCUIT BOARD SIGNAL INTEGRITY

High-Speed Circuit Board Signal Integrity

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High-Speed Circuit Board Signal Integrity

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To Ann, Christopher, and Kevin

Contents

Preface

This is a book for engineers designing high-speed circuit boards. To the signal integrity engineer, this book will be a handbook of formulas and terminology as well as a refresher of basic electrostatic and electromagnetic principals. The high-speed circuit designer will find this book an easy entry into the electromagnetics and physics of high-speed signaling. It introduces concepts fundamental to high-speed signaling, such as lossy transmission line behavior, skin effect, and the characteristics of laminates and surface mount capacitors. The focus throughout is on the effects of dielectric and conductor loss on signal quality, with a particular emphasis on serial differential signaling. Coupling between transmission lines (especially in the context of crosstalk and odd/even modes) is discussed. Besides being useful in serial signaling, this has application to multiconductor busses.

Reflections on transmission lines are only superficially covered in this text. This topic has been extensively covered in the literature, and the reader of this book is assumed to be familiar with the creation and mitigation of reflections on transmission lines. However, the proper routing and termination of differential pairs has not been as well covered in the literature and so is discussed in Chapter 8.

Similarly, power supply decoupling has been thoroughly discussed elsewhere, so the coverage in this book is brief. Instead, the focus here is on managing return paths (something often not well covered) and the electrical characteristics and behavior of capacitors. The material in Chapter 10 is a concise catalog of essential electrical characteristics of discrete capacitors, with a focus on surface mount technology.

The fundamentals of resistance, capacitance, inductance, and loss calculations presented in Chapters 2–5 are illustrated with practical worked examples that may be used as templates to solve similar problems.

Many simple formulas are presented to allow hand calculation of resistance, capacitance, inductance, and impedance. These types of calculations are helpful in developing intuition and in approximating beforehand the results to be expected from field solving software, circuit simulation tools, and laboratory measurements.

Extensive references are given at the end of each chapter, providing the interested reader the opportunity to dig deeper. The references intentionally span classic, older works (some of which were written in the 1950s, but most of the older ones are from the 1960s and 1970s) as well as modern works. The older references are valuable, as they are the original works often cited by others, sometimes without the proper context. Although long out of print, the selected older references are generally available secondhand and are worthy additions to the signal integrity engineer's library. Particular mention is made of Johnson's *Transmission Lines and Networks*

(published in 1950, referenced in Chapter 2) and Skilling's *Electrical Engineering Circuits* (1965, see the references in Chapter 3) and *Transient Electric Currents* (1952). These books are succinct and in my view remain unmatched. Miner's *Lines and Electric Fields for Engineers* (1996, first referenced in Chapter 3) is the one electromagnetics textbook every signal integrity engineer should have in his or her library.

I'm indebted to my friends and coworkers for their support, encouragement, and help during the creation of this book. Special mention must be made of the assistance, perspective, and advice provided by my colleagues Jeff Cooper, Ernie Grella, and Tim Haynes. Special thanks also goes to Fahrudin Alagic for his many months of precise laboratory measurements that support the material appearing in Chapters 5–7. I'm grateful to all of those who suffered through early versions of the manuscript for their constructive remarks. I'm also obliged to the anonymous reviewer for his insightful comments. All of these comments were most helpful and have resulted in an improved text. Of course, any inaccuracies or errors that made it into the text are my doing and in no way reflect on the reviewers.

Finally, I'm especially grateful to my wife Ann for her understanding, patience, encouragement, and unflagging support throughout the many long hours it took to create this work. This book would not have been possible without her.

CHAPTER 1

Characteristics and Construction of Printed Wiring Boards

1.1 Introduction

This is a book about high-speed signaling on printed wiring boards (PWBs). The physical construction of PWBs determines the conductor's resistance (discussed in Chapter 2), its self capacitance (covered in Chapter 3) and inductance (Chapter 4), and the coupling to neighboring conductors (Chapters 5 and 9). At the high frequencies of interest in this book, these electrical primitives appear on a PWB as distributed rather than lumped elements, giving rise to transmission line behavior.

It is thus necessary for the high-speed circuit designer to have an understanding of how PWBs are constructed and a sense of the trade-offs fabricators must make when manufacturing high-density, high-layer count PWBs. This chapter summarizes those characteristics impacting the electrical characteristics of PWBs and introduces some of the terminology used in the PWB design industry.

The larger PWB fabricators provide *design for manufacturability* (DFM) documents (see [1, 2] to cite just two examples) that detail the dimensional and many of the practical requirements necessary to create PWB artwork for their facility. These documents are helpful in understanding the practical state of the art in such things as via size, layer count, and trace width and spacing and can act as a primer to those unfamiliar with PWB technology. Additional underlying detail that is somewhat general in nature may be found in [3, 4].

1.2 Unit System

The PWB industry nearly universally uses an inched-based measuring system rather than the metric system. Trace width and length and dielectric thickness are thus specified in decimal fractions of an inch, as are most component dimensions. However, many micopackage dimensions (most notably the pin or ball pitch) are specified with metric millimeters, and the trace thickness is specified in ounces (relating to the amount of copper plating, as described in Section 1.4). The Appendix tabulates some common conversion factors, but here it's noted that 1m = 39.37008$\overline{}$ in and 1 mil = 0.001 in. Therefore, 1 mil = 0.002539$\overline{}$ ~ 0.00254 cm = 0.02539$\overline{}$ ~ 0.0254 mm.

Example 1.1

A ball grid array micropackage (BGA) has solder balls on a 1-mm pitch. What is the pitch in mils?

Solution

Referring to Appendix A, to convert from inches to millimeters, the value in inches is multiplied by 25.4. The 1-mm ball pitch therefore is equivalent to: $\frac{1 \text{ mm}}{25.4 \text{ mm/in}} = 39.37 \times 10^{-3}$ in = 39.37 mils. As there are not precisely 39.37 in per meter, the conversion factor is not precisely 25.4 mm/in. This error is often inconsequential but can be important over large distances.

1.3 PWB Construction

The typical multilayer PWB is formed as a stack of alternating layers of prepreg mats and laminate sheets. The general idea is shown in Figure 1.1.

The prepreg mats are a weave of glass fiber yarns preimpregnated (hence *prepreg*) with a resin that is intentionally allowed to only partially cure. The sheets come in many stock sizes and yarn *styles* (classified by the number and diameter of the glass threads, the weave, and the percentage of resin impregnation) and serve to strengthen the resin. The typical resin content of the mats is in the 45% to 65% range.

Copper foil is attached to one or both sides of fully cured prepreg sheets to form the laminate sheets (also called *cores*). Similar to the prepreg mats, cores come in standard stock sizes and thicknesses, from which the fabricator must choose to construct a PWB. It's common for outer layers (such as layers L1 and L6 in Figure 1.1) to be formed on prepreg [1], but some manufacturers prefer to form the outer layers on cores.

To form the composite PWB structure, a stackup of prepreg mats and laminate cores are heated under pressure. This causes the partially cured prepreg to flow and bond to the cores. The prepreg cures are cooled, thereby forming the completed PWB structure.

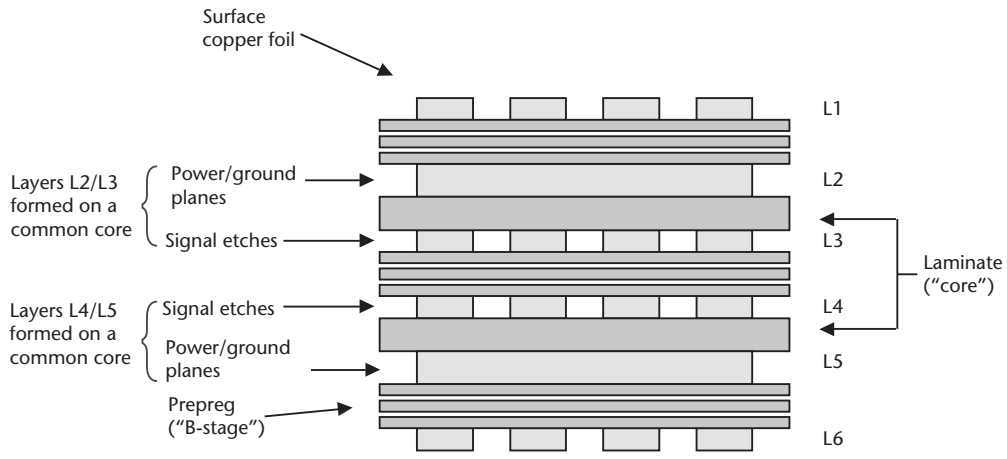

Figure 1.1 Multilayer PWB stackup.

1.3.1 Resins

Several resin systems are used to form prepreg and laminate sheets, with the FR4 epoxy resin system probably being the most popular.

The generic specification *FR4* refers to a specific fire-retardant level rather than to a specific laminate chemistry. The term *standard FR4* is a misnomer: Fabricators have many laminate systems from which to choose that meet FR4 fire specifications, each with unique electrical and mechanical characteristics. Fabricators select the laminate system based on assembly issues (especially temperature extremes) and their history with a particular laminate for a given set of electrical requirements.

The FR4 epoxy can be blended with tetrafunctional or multifunctional resins [5, 6] to improve the material's mechanical characteristics, most notably the coefficient of expansion, the *glass transition temperature*, and the rate of moisture absorption [5].

The coefficient of expansion in height—that is, the *Z* axis, *CTE(Z)*—is an indication of how much the board will enlarge and contract in thickness with temperature changes. Increasing the resin's temperature above its glass transition temperature (Tg) causes the resin to change from its crystalline state to a more fluid, glassy state. Additionally, CTE(Z) is not constant across temperature: increasing temperature above Tg results in a rapid increase in CTE(Z) [7].

Fabricators will recommend the use of a *high Tg* laminate (those with Tg greater than about 180°C [5]) if the PWB will be exposed to high temperatures during assembly or rework operations. This is important because thermally induced stresses can lead to plated through hole failures (see Section 1.5), especially in thick boards having a large CTE(Z).

The drilling operation is another consideration for the fabricator when choosing a laminate. The typical FR4 resin system is relatively easy to drill. High Tg laminates tend to be harder and more brittle, making drilling more difficult. On the other hand, high-speed drilling of vias may warrant the use of a high Tg material to avoid *drill smear*. This is a result of a softening of the laminate near the hole due to drilling induced local heating that momentarily raises the temperature above Tg (Tg ~ 130°C for FR4 [5]).

1.3.2 Alternate Resin Systems

Resins other than the standard FR4 epoxy types are available to form PWB laminates and prepregs. These alternate systems have higher Tg than the tetrafunctional or multifunctional FR4 resins, and superior electrical characteristics. Of principal interest are the values for the dielectric constant (ε_r discussed in Chapter 3) and loss tangent (a parameter describing the amount of energy lost in the dielectric at a specific frequency, also discussed in Chapter 3).

Some of the alternate resin systems include GETEK® (a registered trademark of General Electric Company), MEGTRON® (a registered trademark of Matsushita Electronic Materials), BT (a blend of bismaleimide/triazine such as Allied Signals G200 [8]), polyamide, and cyanate ester resins. As with the FR4 epoxies, these resins are reinforced with glass or other fibers.

GETEK and MEGTRON are blends of polyphenylene oxide and high Tg epoxy reinforced with E glass [9, 10]. These laminates have lower ε_r and loss tangent values than FR4 systems and a lower CTE(Z).

A blend of bismaleimide and cyanate ester resins commonly called BT was originally introduced by Mitsubishi Gas and Chemical Company but is now available from several laminate vendors. This resin system has electrical characteristics somewhat superior to FR4 and is used extensively in the micropackaging industry due to its higher Tg and superior moisture absorption qualities.

Polyamide resins generally have lower ε_r and loss tangent values than FR4 resins and have a significantly higher Tg. These desirable characteristics are somewhat offset by polyamide's affinity for moisture. The ability of these laminates to withstand high temperatures suits them to aerospace applications and commercial test equipment, such as burn-in chamber circuit boards where semiconductors are life tested at high temperatures. Polyamide is also extensively used in the flexible circuit board industry.

Cyanate ester resins have superior electrical characteristics to polyamide and exhibit lower moisture uptake. They are often used in RF applications, but this material is not as suited as other materials to form multilayer stackups [11], so they are not as popular in high-speed digital design work.

The RO4000® series laminates from Rogers Corporation are reinforced hydrocarbon/ceramic materials that are finding increasing use in high-speed digital signaling. These materials have a very high Tg, low loss tangent, and a stable ε_r up to at least 10 GHz [12].

A synopsis of these resin systems in laminate form as represented by Nelco Park [13], Isola-USA [14], Matsushita, and Rogers Corporation appears in Table 1.1. A more complete listing showing various laminate systems from several vendors appears in Chapter 3.

As shown, the multifunctional FR4 epoxies have the lowest Tg and highest ε_r/loss tangent values. Of the resins, polyamide has the highest Tg and ε_r/loss tangent values, second to the cyanate ester resin system. The Rogers RO4350® has the highest Tg and lowest ε_r and loss tangent value.

Table 1.1 Alternate Laminate Systems

Trade Name	*Chemistry*	*Tg*	*ε_r/loss tan*	*ε_r/loss tan*	*Vendor*
		C°	1 MHz	1 GHz	
N7000-1	Polyamide	260	4.3/0.013	3.7/0.007	Nelco
P97	Polyamide	260	4.4/0.014	4.2/0.014	Isola
N8000	Cyanate Ester	250	3.8/0.008	3.5/0.006	Nelco
N5000	BT	185	4.1/0.013	3.8/0.010	Nelco
G200	BT	185	4.1/0.013	3.9/0.009	Isola
N4000-6	Multifunctional	180	4.4/0.023	3.9/0.012	Nelco
Megtron	PPO/Hi Tg Epoxy	180	3.8/0.010	3.75/0.011	Matsushita
FR404	Multifunctional	150	4.6/0.025	4.25/0.014	Isola
RO4350	Ceramic	>280		3.48/0.004 (10GHz)	Rogers

1.3.3 Reinforcements

Fibers (usually from a form of glass) are used to strengthen the resins, but adding them changes the electrical and mechanical characteristics of the composite structures roughly in proportion to the amount of fiber to resin (the *glass-to-resin ratio*). As shown in Table 1.2, the glass fibers have a higher ε_r but superior loss tangent values than the resins.

High glass content improves the composite's CTE(Z), thereby helping to prevent via cracking during high-temperature assembly and rework operations. However, a high glass content increases ε_r and lowers the loss tangent [15, 21]. Generally, higher ε_r is a disadvantage in high-speed PWBs, as that increases capacitive coupling between conductors and tends to result in thicker stackups for a given impedance. Alternatively, for a given stackup thickness, higher ε_r results in narrower trace widths, thereby increasing conductor loss (described in Chapters 2 and 5). Lower loss factors are advantageous, as they improve high-frequency signal qualities (as described in Chapters 3, 5, and 7).

The relationship between resin content and ε_r is generalized in Figure 1.2 for FR4.

The prepregs aggregate ε_r value approaches that of the just the resin for low glass-to-resin ratios and approaches that of the glass itself as more glass is added and the glass-to-resin ratio increases. Figure 1.2 points out the difficulty in judging between laminates simply by comparing published ε_r values, as some manufacturers specify a "worst case" ε_r (i.e., low resin content) while others publish an ε_r corresponding to a higher resin content value (often 50%).

Various glass fiber types are available to reinforce the resin. The most common is *E* glass (electrical grade), which is commonly used throughout the plastics industry. This glass fiber was specifically designed for electrical use, but its versatility has made it suitable for reinforcing a range of plastics. This broad adoption beyond use in the PWB industry is responsible for the low cost of E glass [4]. It primarily consists of silicon oxide, aluminum oxide, and calcium oxide.

Table 1.2 Resin and Reinforcement Properties at 1 MHz

Material	ε_r	*Loss*	*CTE(Z) Parts Per Million (PPM)/C°*	*Moisture Absorption*
				(%)
E Glass	6.2	0.004	5.5	
S Glass	5.2	0.003	2.6	
Thermount®	3.9	0.015	–4.5	0.44
FR4 epoxy resin	3.6	0.032	85	0.7
BT resin	3.1	0.003		
Polyamide resin	3.2	0.02	50	0.9
Cyanate Ester resin	2.8	0.002	50	0.5

Source: [4, 7, 15–20].

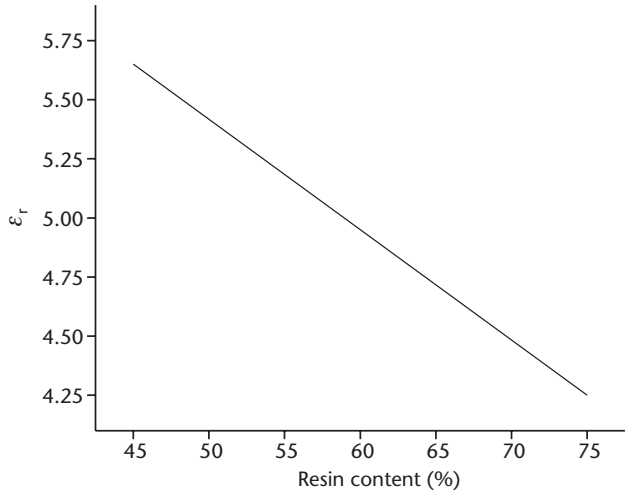

Figure 1.2 Relationship between resin content and ε_r for FR4.

A second glass fiber finding increasing use in PWBs is *S* glass (structural grade). This glass fiber was specifically developed for high-strength reinforcement applications and also consists of silicon oxide and aluminum oxide, but it uses magnesium oxide in place of the calcium oxide [6]. It's stronger than E glass and has a lower ε_r, but it's not as widely used and so is more expensive (about four times that of E glass [6]).

A nonwoven Aramid fiber called Thermount [17] is finding increasing use as a reinforcement to epoxy, polyamide, cyanate ester, or Teflon® resins in PWB applications. Thermount is comprised of very short *Kevlar*® fibers [5]. It offers lower ε_r than either E or S glass and has a negative CTE(Z), which can be advantageous in reducing the expansion of the composite structure [4]. Thermount, Kevlar, and Teflon are registered trademarks of E. I. Dupont de Nemours & Co., Inc.

1.3.4 Variability in Building Stackups

In producing a multilayer PWB as depicted in Figure 1.1, the fabricator must decide on the thickness of the laminate and the styles, thickness, and the number of prepreg mats to use to form each layer. The laminate sheets tend to have lower resin content than the prepreg, so the laminates usually have higher ε_r than the prepreg sheets. The way in which the fabricator chooses to form the stackup is fundamental in that it determines ε_r and the loss tangent for a particular layer. One fabricator may choose to use several thin, high-resin-content mats resulting in a lower overall ε_r, while another prefers to use a single, thicker mat having lower resin content which will yield a higher ε_r to get the same overall thickness.

The vendor's latitude in making all of these choices means that ostensibly identical PWBs fabricated by different vendors will quite naturally have different electrical properties. These trade-offs are discussed in Chapter 9.

1.3.5 Mixing Laminate Types

It's not necessary for the cores to all be the same laminate material. Historically this hybrid-type construction has been expensive and not widely used in the commercial digital PWB industry, but in recent years it's become somewhat more mainstream. In spite of its fabrication complexity, it can be cost effective to use a lower cost, lower performance laminate throughout most of the stackup and strategically mix in a few expensive, higher performance layers only where needed. This is especially attractive for stackups that have many layers, where only a few carry high-frequency, loss-sensitive signals. In these situations, the complexity of fabricating a stackup containing different materials costs less than making the high layer count stackup entirely from the high-performance, expensive laminate. The materials chosen must have similar CTE values [22, 23] so not all laminate types can be mixed.

Also note that the copper thickness need not be the same throughout the stackup. Having different copper thickness on various layers is common in situations where the power/ground planes must be thick for proper power supply distribution but the signal traces need not be. As described in Chapter 2, at high frequency the skin effect causes signal currents to migrate to the conductor's surface. This means thick traces do not necessarily have a loss advantage over thinner ones. An additional advantage of using thin copper for signal traces is that it's easier to retain a truly rectangular shape when etching the thinner copper. This has loss, coupling, and impedance advantages (see Chapter 9). Using thinner copper for the signal traces can help reduce the stackup's thickness, but using thin copper for the power/ground planes reduces their ability to wick heat from the pins of an integrated circuit or field effect transistor (FET) (as is found in switching power supplies or when FETS are used in power supply sequencing circuits).

To avoid warpage, manufacturers favor *balanced* stackups, where the thin and thick layers are distributed symmetrically about the stackup's center, but this also applies to the distribution of laminate types.

1.4 PWB Traces

Copper traces are used to form the PWB conductors, either of the board's surface (*microstrip* or *embedded microstrip*) or buried within the PWB as *stripline* (see Figure 1.3).

To properly model high-frequency conductor losses, it's important for the high-speed circuit designer to understand the process used to form a trace. The

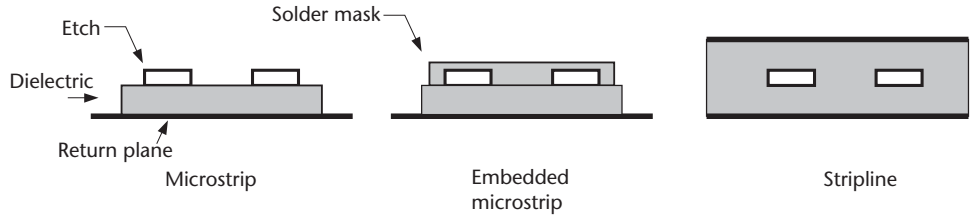

Figure 1.3 Microstrip and stripline defined.

nature of the multilayer PWB fabrication process is such that the mechanical characteristics of the inner layer copper is different from the copper on the board's outer surfaces. The outer layers are plated, while the inner ones are not. Copper cladding is discussed in this section. Plating and the consequences to outer layer conductors are discussed in Sections 1.4.2 and 1.6.

1.4.1 Copper Cladding

The copper cladding attached to laminate sheets is created by either an electrodeposition or rolling process [24, 25]. These processes create copper foils with different surface roughness. As is shown in Chapter 2, accounting for surface roughness is important when computing skin effect losses.

The electrodeposited process (ED) creates copper foil by a plating process that forms a copper sheet by extracting copper from solution onto a rotating drum [26]. The foil side in contact with the drum is smoother than the other surface. In contrast, the rolling process starts with a copper ingot that is passed through rollers multiple times until it is reduced to the desired thickness. This process creates foil equally smooth on both sides, and smoother than that of electrodeposited copper. A smooth surface is advantageous when signaling at high frequency because (as explained in Chapter 2) the ac resistance will be lower with a smooth surface than it will be with a rough one. This makes rolled copper trace electrically preferred over ED at high frequencies. However, the greater coarseness of ED foil allows the copper to better adhere to the substrate, giving ED foils higher *peel strengths*. Foils with higher peel strengths have better adhesion and so are less likely to lift off from the laminate during soldering or rework operations.

To promote adhesion with the laminate material, both types of foils are roughened on one side (or sometimes both sides) to increase surface area. There are many techniques available for fabricators and laminators to use [27], each producing different copper grain sizes and shapes. Surface roughness is measured as the root-mean-square (RMS) height of the irregularity above the surface.

As shown in Table 1.3, in general, even after processing, rolled copper has a lower surface roughness than ED.

The data in Table 1.3 should only be taken as representative. Actual values depend on processing and will vary between manufacturers.

Because the CTE of copper foil is actually lower than that of the laminate, thermally induced stresses can cause the connection to a via to fracture over time or with repeated thermal cycling. High-temperature elongation (HTE) foils can be used to mitigate this susceptibility to stress [28]. These foils are also sometimes called *class 3 foils* after the Institute for Interconnecting and Packaging Electronic Circuits (IPC) industry standards group designation [29]. Foils in this category have a higher CTE

Table 1.3 Typical Copper Foil Characteristics

	Average Thickness (mils)	*ED μ-inches (RMS)*	*Rolled (Treated Side) μ-inches (RMS)*
Half ounce	0.65	75–100	50–60
One ounce	1.4	95	50–60

Source: [24, 25].

than the *class 1 foils* that are in general use and more closely match the laminate's CTE. The use of HTE foils is becoming common, especially on higher performance resin-based laminates, but they are generally not used with laminate systems having a low CTE(Z), such as the Rogers 4000® series materials.

1.4.2 Copper Weights and Thickness

The thickness of the copper foil is usually specified by its nominal weight in ounces per square foot of area. Table 1.4 shows the relationship of weight to nominal and minimum thickness as specified by the IPC [21].

Notice that due to plating, the external conductors (i.e., microstrip) will usually be thicker than the inner layers (stripline) of the same weight.

1.4.3 Plating the Surface Traces

A plating process usually forms surface traces where copper is selectively plated on top of the thin foil present on the PWB's surface. The traces thus formed are protected from the subsequent etching step by coating the traces with either a metal (tin or tin/lead) or a nonconducting photoresist [4]. This is visible in Figure 1.4, which shows the copper trace with a plating material on top of the base copper.

1.4.4 Trace Etch Shape Effects

The shape of the trace is a factor in determining its impedance and resistance, and nearly all hand formulas for computing impedance assume a rectangular trace. Rectangular trace shapes are also usually assumed when field-solving software is used to calculate impedance. However, the etching process attacks the copper both vertically and horizontally, resulting in traces that are roughly trapezoidal in shape. This vertical *over etching* is numerically described by the *etch factor,* which is the ratio of the conductor's thickness to the amount of copper that has been undercut:

$$EF = \frac{t}{uc} \tag{1.1}$$

Referring back to Figure 1.4, t is the trace thickness and uc is the amount the copper trace is undercut on one side [1].

Table 1.4 Relationship Between Copper Weight Specification and Thickness

Weight Specifier (oz)	*Nominal Thickness (mils)*	*Minimum Internal Layer Thickness (mils)*	*Minimum External Layer Thickness (mils)*
$\frac{1}{4}$	0.35	0.25	0.8
$\frac{1}{2}$	0.70	0.50	1.30
1	1.4	1.0	1.8
2	2.8	2.2	3.0