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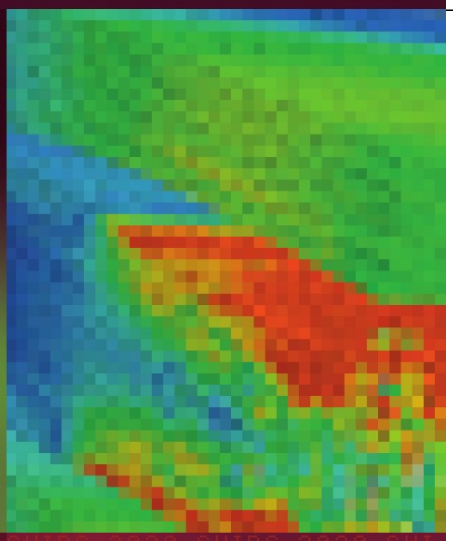

Bernd Hoefflinger (Ed.)

CHIPS 2020

A Guide to the Future of Nanoelectronics

Springer

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Editor

Chips 2020

A Guide to the Future of Nanoelectronics

Springer

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Preface

On July 30, 1959, Robert Noyce filed his Integrated Circuit patent. Its fiftieth anniversary in 2009 became the origin of this book and its central question: After the unparalleled progress of microchips over half a century, can this story continue, and what will it take to make this happen?

To greet the year 2000, I had written an invited paper "Chips 2020" for the German magazine *Elektronik* (with a strong vote for 3D chip integration), and it looked attractive to check the status at half-time, in 2010. However, the central issue of this book emerged owing to more and more signs of the imminent end of the nano(meter) *roadmap*: The law that halving the transistor size every 18 months would bring automatic performance and market growth is about to end in 2015. When the billions of 10 nm$\times$10 nm transistors packed side-by-side on a chip are hardly useful because of their fundamental statistical variance, we face the most important turning point in the history of microelectronics: Declining growth in markets and services and an energy crisis on top, because, with the chip technology of 2010 and with the present annual doubling of video and TV on the internet, this service alone would require the total worldwide electrical power in 2015.

Chips 2020 explains the background to the 20–10 nm transistor limits in different applications, and it focuses on the new strategy for the sustainable growth of a nanoelectronics ecosystem with a focus on ultra-low energy of all chip functionalities, femtojoule electronics, enabled by 3D integration on-chip and of chip-systems incorporating new architectures as well as new lithography and silicon technologies.

At the critical time of this new fundamental energy orientation, I have been very fortunate that several world leaders with their teams agreed to contribute to this book: Greg Delagi of Texas Instruments, on intelligent mobile companions, the new lead products; Georg Kimmich of ST-Ericsson, on 3D integration for wireless applications; Burn Lin of TSMC, on nanolithography; Jiri Marek and Udo Gomez of Robert Bosch GmbH, on MEMS (micro-electro-mechanical systems) for automotive and consumer applications; Barry Pangrle of Mentor Graphics, on power-efficient design; Peter Roth and colleagues at IBM, on superprocessors; Yiannos Manoli with his team at the University of Freiburg, together with Boris Murmann of Stanford University, on analog–digital interfaces and energy harvesting; Albrecht

Rothermel of the University of Ulm, on retinal implants for blind patients; and Ben Spaanenburg with his co-author at Lund University, on digital neural networks. This book would be unthinkable without their contributions, and, in this critical situation for nanoelectronics, I am even more obliged to them for their involvement in this project.

Despite our broad agenda, we could cover only selected topics, which, we hope, are exemplary for the potential and challenges for 2020 chips.

My sincere thanks go to Claus Ascheron at Springer in Heidelberg, who constantly pursued the idea for this book and who finally convinced me in 2009 to realize it. I thank the team at Springer Science+Business Media for their confidence in this publication and for its professional production. I thank Stefanie Krug for her perfect execution of many of the illustrations and Deborah Marik for her professional editing of the manuscript.

With experience as the first MOS product manager at Siemens and of co-founding a Technical University and establishing several microchip research facilities in the USA and Germany, I have included educational, research, and business aspects of the nanoelectronics ecosystem. I hope that, with this scope, this book will be helpful to all those who have to make decisions associated with future electronics, from students to graduates, educators, and researchers, as well as managers, investors, and policy makers.

Sindelfingen Bernd Hoefflinger

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Biographies of Authors

Greg Delagi has been senior vice president and general manager of TI's Wireless Terminals Business since 2007, where he leads TI's worldwide development of semiconductors for mobile phones. Greg Delagi started his career with Texas Instruments in 1984 with the Materials and Controls Business. He later joined TI's Semiconductor Group. Delagi was responsible for several of the company's business units such as DSL, Cable, VoIP and Wireless LAN, creating systems-on-chip solutions. As vice president and manager of TI's Digital Signal Processing (DSP) business, he guided the company to its world leadership with a 62% share of the world market in 2006. He is a graduate of Nichols College in Dudley, MA, where he earned a BSBA in 1984.

Udo Gómez has been Director of Engineering since 2006 for Advanced Sensor Concepts at Bosch, Automotive Electronics Division, in Reutlingen, Germany, responsible for MEMS sensor predevelopment activities. He also serves as chief expert for MEMS sensors. From 2003 until 2005, he was responsible for the development of a novel automotive inertial sensor cluster platform for active safety applications. Dr. Gómez studied physics at the University of Stuttgart, Germany. In 1997, he received his Ph.D. from the University of Stuttgart for his work on molecular electronics. In January 1998, he joined the California Institute of Technology as a post-doctoral fellow. In 1999, he started his work at Bosch Corporate Research.

Bernd Hoefflinger started his career as an assistant professor in the Department of Electrical Engineering at Cornell University, Ithaca, NY, USA. Returning to Germany, he served as the first MOS product manager at Siemens, Munich. With that background, he became a co-founder of the University of Dortmund, Germany, and later head of the Electrical Engineering Departments at the University of Minnesota and at Purdue University, IN, USA. In 1985, he became the director of the newly established Institute for Microelectronics Stuttgart (IMS CHIPS), a public contract research and manufacturing institute. In 1993, IMS CHIPS became the world's first ISO 9000 certified research institute. He launched rapid prototyping with electron-beam lithography in 1989. He established the institute as a leader in high-dynamic-range CMOS imagers and video cameras from 1993 onwards. Among the developments in CMOS photosensors was the chip design and manufacturing for the first sub-retinal implants in humans in Europe in 2005. He retired in 2006.

Christian Jacobi received both his M.S. and Ph.D. degrees in computer science from Saarland University, Germany, in 1999 and 2002, respectively. He joined IBM Research and Development in 2002, working on floating-point implementation for various IBM processors. For IBM's System z10 mainframe, he worked on the L1.5 cache unit. From 2007 to 2010, Dr. Jacobi was on international assignment to Poughkeepsie, NY, where he worked on the Load-Store-Unit for the IBM zEnterprise 196 mainframe. Dr. Jacobi is now responsible for the cache design of IBM's mainframe processors, and for future architecture extensions.

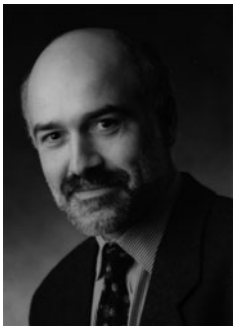
Matthias Keller was born in Saarlouis, Germany, in 1976. He received his Diploma degree in electrical engineering from the University of Saarland, Saarbrücken, Germany, in 2003 and a Dr.-Ing. degree (summa cum laude) from the University of Freiburg, Germany, in 2010. From 2003 to 2009, he was a research assistant at the Fritz Huettinger Chair of Microelectronics at the University of Freiburg, Germany, in the field of analog CMOS integrated circuit design with an emphasis on continuous-time delta-sigma A/D converters. In 2009, he was awarded a tenured position as a research associate ("Akademischer Rat"). His research interests are analog integrated circuits based on CMOS technology, in particular delta-sigma A/D converters and patch-clamp readout circuits.

Georg Kimmich is product manager at ST-Ericsson in Grenoble, France. He is responsible for the product definition of digital baseband system-on-chip products within the 3G Multimedia and Platform Division. His focus is on the technology roadmap definition for chip packaging. Georg Kimmich graduated in computer engineering at HFU, Furtwangen, Germany in 1990. He held several design and management positions in the design automation and ASIC design domain with Thomson Multimedia and STMicroelectronics in Germany, France and the US. In 2006, he joined the application processor division of STMicroelectronics, where he was responsible for the system-on-chip development team of the Nomadik application processor family.

Burn J. Lin became a vice president at TSMC, Ltd., in 2011. He joined TSMC in 2000 as a senior director. Prior to that, he founded Linnovation, Inc. in 1992. Earlier he held various technical and managerial positions at IBM after joining IBM in 1970. He has been extending the limit of optical lithography for close to four decades. He pioneered many lithography techniques, among them deep-UV lithography starting from 1975, multi-layer resist from 1979, Exposure-Defocus methodology from 1980, k_1 reduction from 1987, attenuated phase-shifting mask from 1991, 193 nm immersion lithography from 2002, and polarization-dependent stray light from 2004. He is currently working on cost-effective optical lithography and multiple-electron-beam mask-less lithography for the 20 nm node and beyond.

Dr. Lin is the editor-in-chief of the *Journal of Micro/nanolithography, MEMS, and MOEMS*, life member of the US National Academy of Engineering, IEEE Life Fellow, and SPIE Fellow. He has received numerous awards, among them the 1st Semi IC Outstanding Achievement Award in 2010, the 2009 IEEE Cledo Brunetti Award, the 2009 Benjamin G. Lammé Meritorious Achievement Medal, and in 2004 the 1st SPIE Frits Zernike award. Throughout his career, he has received numerous TSMC and IBM Awards. He has written one book and three book chapters, published 121 articles, mostly first-authored, and holds 66 US patents.

Suleyman Malki received, in October 2008, a Ph.D. degree from the Department of Electrical and Information Technology at Lund University for work on the topic "Reconfigurable and Parallel Computing Structures in Structured Silicon". Before that he received a master's degree in computer science and engineering from Lund University. His research has focused mainly on the implementation and verification of highly intelligent systems on reconfigurable chips (FPGA). Currently he is devoting most of his time to his recent biological and industrial offspring.



Yiannos Manoli was born in Famagusta, Cyprus. As a Fulbright scholar, he received a B.A. degree (summa cum laude) in physics and mathematics from Lawrence University in Appleton, WI, in 1978 and a M.S. degree in electrical engineering and computer science from the University of California, Berkeley, in 1980. He obtained a Dr.-Ing. degree in electrical engineering from the University of

Duisburg, Germany, in 1987. From 1980 to 1984, he was a Research Assistant at the University of Dortmund, Germany. In 1985, he joined the newly founded Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany. From 1996 to 2001, he held the Chair of Microelectronics with the Department of Electrical Engineering, University of Saarbrücken, Germany. In 2001, he joined the Department of Microsystems Engineering (IMTEK) of the University of Freiburg, Germany, where he established the Chair of Microelectronics. Since 2005, he has additionally served as one of the three directors at the "Institute of Micromachining and Information Technology" (HSG-IMIT) in Villingen-Schwenningen, Germany. He spent sabbaticals with Motorola (now Freescale) in Phoenix, AZ, and with Intel, Santa Clara, CA. Prof. Manoli has received numerous best paper and teaching awards, and he has served on the committees of ISSCC, ESSCIRC, IEDM and ICCD. He was Program Chair (2001) and General Chair (2002) of the IEEE International Conference on Computer Design (ICCD). He is on the Senior Editorial Board of the IEEE *Journal on Emerging and Selected Topics in Circuits and Systems* and on the Editorial Board of the *Journal of Low Power Electronics*. He served as guest editor of *Transactions on VLSI* in 2002 and *Journal of Solid-State Circuits* in 2011.

Jiri Marek has been Senior Vice President of Engineering Sensors at Bosch, Automotive Electronics Division, since 2003, responsible for the MEMS activities at Bosch. He started his work at Bosch in 1986. From 1990 until 1999, he was responsible for the Sensor Technology Center. In 1999, he became Vice President Engineering of Restraint Systems and Sensors. Dr. Marek studied Electrical Engineering at the University of Stuttgart, Germany, and Stanford University, USA. In 1983, he received his Ph.D. from the University of Stuttgart for his work at the Max Planck Institute Stuttgart on the analysis of grain boundaries in large-grain polycrystalline solar cells. After a post-doctoral fellowship with IBM Research, San José, CA, he was a development engineer with Hewlett-Packard, Optical Communication Division.

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Barry Pangrle is a Solutions Architect for Low Power in the Engineered Solutions Group at Mentor Graphics Corporation. He has a B.S. in computer engineering and a Ph.D. in computer science, both from the University of Illinois at Urbana-Champaign. He has been a faculty member at University of California, Santa Barbara and Penn State University, where he taught courses in computer

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Peter H. Roth received his Dipl.-Ing. degree in electrical engineering and his Dr.-Ing. degree from the University of Stuttgart, Germany, in 1979 and 1985, respectively. In 1985, he joined the IBM Germany Research and Development Lab in Boeblingen, starting in the department of VLSI logic-chip development. Since 1987 he has been leading the VLSI test and characterization team of the Boeblingen lab. Later, Dr. Roth led several development projects in the area of IBM's Mainframe and Power microprocessors. He also was heavily involved in the development of gaming products such as the Cell processor for the Sony PlayStation. Today, Dr. Roth is responsible for the hardware strategy for the IBM Germany Research and Development Laboratory.

Albrecht Rothermel received his Dipl.-Ing. degree in electrical engineering from the University of Dortmund, and his Dr.-Ing. (Ph.D.) degree from the University of Duisburg, both Germany, in 1984 and 1989, respectively. From 1985 to 1989, he was with the Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany. From 1990 to 1993, he was with Thomson Consumer Electronics (Thomson Multimedia), Corporate Research, Villingen-Schwenningen, Germany. As manager of the IC design laboratory, he was involved in analog and mixed circuit design for audio and video. Since 1994, he has been with the Institute of Microelectronics, University of Ulm, Germany, as a Professor of Electrical Engineering. Dr. Rothermel was a guest scientist at Thomson Multimedia in Indianapolis, USA (1997), at the Edith-Cowan University in Perth, Western Australia (2003), and at the Shandong University in Jinan, P.R. China (2006). He has published more than 100 papers, book chapters, and patents and received numerous best-paper awards. He was an Associate Editor of the *IEEE Journal of Solid-State Circuits*, and he is a member of the program committees of ISSCC, ESSCIRC, and ICCE. He is a senior member and distinguished lecturer of the IEEE.

Lambert Spaanenburg received his master's degree in electrical engineering from Delft University and his doctorate in technical sciences from Twente University, both in The Netherlands. He started his academic journey at Twente University in the field of VLSI design, eventually serving as CTO of ICN, the commercial spin-off of the ESPRIT Nelsis project. At IMS in Stuttgart, he co-created the neural

control for the Daimler OSCAR 1992 prototype, currently an upcoming standard for car safety measures. He became a full professor at the University of Groningen, The Netherlands. Further research of his group in neural image processing led in 2002 to Dacolian, which held a 60% market share for license-plate recognition before it merged into Q-Free ASA. Overall, Dr. Spaanenburg has produced more than 200 conference papers, 20 reviewed journal articles and seven books or chapters. He has served annually on several program committees and journal boards. He has been involved in many technology transfer projects, including eight university spin-offs. Currently a guest at Lund University, he is exploiting further research on embedded sensory networks with cloud connectivity under the umbrella of RaviteQ AB in Sweden.

Kai Weber received his Dipl.-Ing.(BA) in information technology from the University of Collaborative Education, Stuttgart, and a bachelor degree in computer science from the Open University, UK, in 2003. He joined IBM Research and Development in 2003, working on formal verification of floating-point units and leading the floating-point unit verification teams for IBM's POWER6 and z10 processors. Mr. Weber was the processor verification team leader for the IBM zEnterprise 196 mainframe and continues in this role for future generations of IBM System z processors. In addition Mr. Weber is participating in two joint research projects with the University of Tuebingen and Saarland University evaluating hybrid systems and business analytic workloads.

Acronyms and Abbreviations

AAEE	American Association for Engineering Education
AC	Alternating current
ACM	Association for Computing Machinery
ADC	Analog–digital converter
AI	Artificial intelligence
ALE	Atomic-layer epitaxy
ALU	Arithmetic logic unit
AMD	Age-related macula degeneration
ANN	Artificial neural network
AP	Action potential
APS	Active-pixel sensor
APSM	Advanced porous silicon membrane
AQL	Acceptable quality level
ARPA	Advanced Research Projects Agency
ASIC	Application-specific integrated circuit
ASIP	Algorithm-specific integrated processor
ASP	Application-specific processor
ASS	Application-specific system
AVG	Available voltage gain
AVS	Adaptive voltage scaling
BAN	Body-area network
BAW	Bulk acoustic wave
BEOL	Back-end of line
BI	Backside illumination
BiCMOS	Bipolar CMOS
BIST	Built-in self-test
BMI	Brain–machine interface
BST	Boundary-scan test
C4	Controlled-collapse chip connect
CAD	Computer-aided design
CAM	Content-addressable memory
CARE	Concerted Action for Robotics in Europe

CAT	Computer-aided test
CCD	Charge-coupled device
CDMA	Code-division multiple access
CE	Continuing education
CFC	Chip-integrated fuel cell
CIFB	Cascade of integrators in feedback
CIFF	Cascade of integrators in feed-forward
CIS	Charge-integration sensor
CISC	Complex-instruction-set computer
CMOS	Complementary metal–oxide–semiconductor
CNN	Cellular neural network
CNT	Carbon nanotube
COO	Cost of ownership
CORDIC	Coordinate rotation digital computer
CPU	Central processing unit
CSF	Contrast-sensitivity function
CT-CNN	Continuous-time CNN
DA	Design automation
DAC	Design-Automation Conference
DAC	Digital–analog converter
DARPA	Defense Advanced Research Projects Agency
DBB	Digital baseband
dBm	Power on a log scale relative to 1 mW
DC	Direct current
DCF	Digital cancelation filter
DDR2	Dual data rate RAM
DEM	Dynamic element matching
DFT	Design for test
DIBL	Drain-induced barrier lowering
DIGILOG	Digital logarithmic
DLP	Digital light processing
DMA	Direct memory access
DN	Digital number
DNN	Digital neural network
DPG	Digital pattern generator
DPT	Double-patterning technology liquid-immersion lithography
DRAM	Dynamic random-access memory
DRIE	Deep reactive-ion etching
DSP	Digital signal processor
DT-CNN	Discrete-time CNN
DTL	Diode–transistor logic
D-TLB	Data-cache translation lookaside buffer
DVFS	Dynamic voltage and frequency scaling
EBL	Electron-beam lithography

ECC	Error-correcting code
ECG	Electrocardiogram
ECL	Emitter-coupled logic
EDA	Electronic design automation
EEG	Electroencephalography
EITO	European Information Technology Organization
ELO	Epitaxial lateral overgrowth
ELTRAN	Epitaxial-layer transfer
EMI	Electromagnetic interference
ENOB	Effective number of bits
EOT	Equivalent oxide thickness
ERC	Engineering Research Center
ERD	Emerging research devices
ERM	Emerging research materials
ESD	Electrostatic discharge
ESL	Electronic-system level
ESP	Electronic safety package
ESP	Electronic Stability Program
ESPRIT	European Strategic Programme for Research in Information Technology
EUV	Extreme ultraviolet
EWS	Electrical wafer sort
FACETS	Fast Analog Computing with Emergent Transient States
FC	Fuel cell
FD SOI	Fully depleted silicon-on-inulator
FED	Future Electron Devices
FEOL	Front-end of line
FeRAM	Ferroelectric random-access memory
FET	Field-effect transistor
F^2	Square of minimum feature size
FFT	Fast Fourier transform
FIFO	First-in-first-out
FIPOS	Full isolation by porous silicon
FIR	Finite impulse response
FIT	Failure in 10^7 h
FLOP	Floating-point operation
FMEA	Failure mode and effect analysis
FOM	Figure-of-merit
FPAA	Field-programmable analog array
FPGA	Field-programmable gate array
fps	frames per second
FR	Floating-point register
FSM	Finite-state machine
FSR	Full signal range